ABSTRACT OF THE DISCLOSURE

A method and apparatus is provided for replacing defective storage cells within a memory device having twisted bit lines. If a defective storage cell is discovered, the row containing that storage cell can be re-mapped to the neighboring row or the memory array. Each successive neighboring row is also re-mapped to succeeding neighboring rows by incrementing or decrementing the row addresses. This will cause the addresses to essentially shift one address value toward the redundant set of rows, and one redundant row will be subsumed for every defective row within the array. Whenever an address is shifted across a twist region, the data of that address is purposely inverted in binary voltage value (i.e., converted from a binary 1 to a binary 0, and vice versa) to accommodate the twisting of the true and complementary bit line locations.